AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter.

Claims:

1. (Original) A memory unit, comprising:

first and second access transistors coupled to a bit line pair, wherein the first access transistor comprises a first terminal coupled to one bit line pair, and the second access transistor comprises a first terminal coupled to the other;

a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and

a selection unit having two input terminals coupled to a word line and a flush line, and an output terminal coupled to gates of the first access transistor and the second assess transistor, wherein predetermined information is written to the latch node from the bit line pair according to activations of the word line or the flush line.

2. (Original) The memory unit as claimed in Claim 1, wherein the selection unit is an OR gate with two terminals coupled to the word line and the flush line respectively and an output terminal coupled to the gates of the first access transistor and the second access transistor.

3. (Original) The memory unit as claimed in Claim 1, wherein the latch node comprises a first inverter and a second inverter, the first inverter comprises an input terminal coupled to the second terminal of the second access transistor and an output terminal coupled to the second terminal of the first access transistor, and the second inverter comprises an input terminal coupled to the output terminal of the first inverter and an output coupled to the input terminal of the first inverter.

4. (Original) The memory unit as claimed in Claim 1, wherein when the flush line is activated during a flush operation, the first access transistor and the second access transistor are turned on, such that the predetermined information is written into the latch from the bit line pair.

5. (Original) A memory module, comprising:

at least one first memory region comprising a plurality of memory units, each memory unit comprising:

first and second access transistors coupled to a bit line pair, wherein the first access transistor includes a first terminal coupled to one of the bit line pair, and the second access transistor includes a first terminal coupled to the other;

a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and

a selection unit including a first input terminal coupled to a word line, an output terminal coupled to gates of the first access transistor and the second assess transistor, and a second input terminal;

wherein the second input terminals of the selection units in all memory units are coupled to a flush line, and invalidation information is written into the latch nodes in the memory units from the bit line pair when the flush line is activated during a flush operation.

6. (Original) The memory module as claimed in Claim 5, wherein predetermined information is written to latch node of one of the memory units from the bit line pair when a corresponding word line is activated during a normal operation.

7. (Original) The memory module as claimed in Claim 5, wherein the selection unit is an OR gate comprising two input terminal coupled to a corresponding word line and the flush line, and an output terminal coupled to the gate of the first access transistor and the second access transistor.

8. (Original) The memory module as claimed in Claim 5, wherein when the flush line is activated during the flush operation, the first access transistor and the second access transistor are turned on, such that the invalidation information is written to the latch nodes in the first and second memory units from the bit line pair.

9. (Original) The memory module as claimed in Claim 5, wherein the latch node comprises a first inverter and a second inverter, the first inverter comprises an input terminal coupled to a the second terminal of the second access transistor and an output terminal coupled to the second terminal of the first access transistor, and the second inverter comprises an input terminal coupled to the output terminal of the first inverter and an output coupled to the input terminal of the first inverter.

10. (Currently Amended) The memory module as claimed in Claim 5, further comprising:

a D-type Flip-Flop (DFF) receiving and synchronizing a flush signal; and

a driving buffer coupled to the DFF to activate ~~active~~ the flush line according to the flush signal from the DFF.

11. (Currently Amended) A fabricating procedure for a cache memory, comprising:

determining conditions for a tag memory in the cache memory according to a desired specification of the cache memory;

implementing the tag memory as a memory module according to determined conditions, wherein tag memory comprises a plurality of memory units, each comprising:

first and second access transistors coupled to a bit line pair, wherein the first access transistor comprises a first terminal coupled to one bit line pair, and the second access transistor comprises a first terminal coupled to the other;

a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and

an OR gate comprising two input terminals coupled to a word line and a flush line, and an output terminal coupled to gates of the first access transistor and the second assess transistor, wherein invalidation information is written to the all latch nodes in the memory units from the bit line pair according to activation of the flush line;

checking whether the implemented tag memory meets the determined conditions; ~~and~~

implementing peripheral elements in the cache memory according to the desired specification of the cache memory;

modifying the peripheral elements to match the tag memory such that the peripheral elements meet the desired specification; and

simulating integration of the tag memory and the peripheral elements in the cache memory to ensure compliance thereof with the desired specification.

12. (Original) The fabricating procedure as claimed in Claim 11, wherein the conditions comprise the size and the flush cycle time of the tag memory.

13. (Original) The fabricating procedure as claimed in Claim 11, wherein the desired specification comprises a number of entries, a desired speed and desired performance for the cache memory.